REMARKS

This paper is responsive to the Final Office Action dated January 28, 2003, having a shortened statutory period expiring April 28, 2003, in which:

Claims 1-29 were pending; and

Claims 1-29 were rejected.

No claims have been amended, added, or cancelled by this amendment.

Accordingly, Claims 1-29 remain currently pending in the present application.

Rejection of Claims under 35 U.S.C. §102

Claims 1-3, 6, 7, 13-17, 20-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,128,666, issued to Muller et al. (hereinafter, "***Muller***").

Rejection of Claims under 35 U.S.C. §103

Claims 1-7, 13-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claims 1-3, 6, 7, 13-17, 20-22, and 25-27 above, and further in view of United States Patent No. 6,018,524 issued to Turner et al. (hereinafter, "***Turner***").

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 5,761,191 issued to VanDervort et al. (hereinafter, "***VanDervort***").

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 6,275,953 issued to Vahalia et al. (hereinafter, "***Vahalia***").

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 6,078,593 issued to Eames et al. (hereinafter "***Eames***").

While not conceding that any of the Examiner's cited references qualify as prior art, but instead to expedite prosecution, Applicants have chosen to respectfully disagree and traverse the Examiner's responses to Applicants' arguments and rejections as follows. The amendments and arguments herein are made without prejudice to Applicants' right to establish, for example in a continuing application, that one or more of the Examiner's cited references do not qualify as prior art with respect to an invention embodiment currently or subsequently claimed.

In the present Office Action, the Examiner states that, "Applicant defines 'parsing a packet...to determine a vector' in Page 5, lines 1-8" and that "a vector, as used here, is an identifying number or data field." Applicants respectfully submit that the claims are to be interpreted according to their ordinary meaning unless found to be indefinite. As there are no outstanding claim rejections under 35 U.S.C. §112, Applicants submit that the Examiner's reference to Applicants' specification is unnecessary and improper.

In the present Office Action, the Examiner states that, "Applicant added emphasis to the phrase 'if there is' in order to presumably question this aspect. Examiner clarifies by responding that not every packet that passes through the system has to be parsed, or requires a header update, and the system is set up to handle these eventualities (col. 6, lines 19-22). More information can be shown in Fig. 3-6, with special emphasis on Fig. 5, #515-520." Applicants respectfully disagree. In the prior Office Action, having a mailing date of August 19, 2002, the Examiner cited ***Muller***, Column 6, lines 5-10 as teaching "parsing a packet, said packet having a header portion, to determine a vector" as claimed by Applicants. By placing emphasis on "if there is", Applicants intended to indicate that the previously-cited portion of ***Muller*** teaches, at most, a determination of **whether or not** information relevant to the packet such as type of packet is present within database 320, consequently resulting in an indication (e.g., "yes" or "no") rather than a determination of "a vector" as claimed.

In the present Office Action, the Examiner has cited additional portions (Abstract, Lines 6-7; Column 1, Line 65 – Column 2, Line 2; Column 6, Lines 10-12) as showing or describing "parsing a packet, said packet having a header portion, to determine a vector" as claimed by Applicants and further stated that, "In this teaching, the search engine 315 acts as a packet parser, because it looks at the header, and then uses the database to determine category information." Applicants respectfully disagree. The Examiner's cited portions of ***Muller*** teach a

search engine which searches a database maintained on a switch element to determine "the type of packet, e.g., VLAN supported or whether the packet can be routed" and that, "it is contemplated that a variety of configurations of search engines and databases may be used."

Applicants respectfully submit however that ***Muller*** fails to teach, show, or suggest, "parsing a packet, said packet having a header portion, to determine **a vector**" as claimed. (Applicants' claim 1, emphasis supplied) Moreover, Applicants can find no teaching of "category information" within the cited portions of ***Muller*** as suggested by the Examiner. Given the ordinary meaning of the term "vector" and absent, at the very least, some suggestion or motivation of the determination of "a vector", either in the Examiner's cited references or in the knowledge of one of ordinary skill in the art at the time of Applicants' invention, Applicants respectfully submit that claim 1, as presented, is allowable over ***Muller***.

In the present Office Action, the Examiner states that, "Applicant teaches that peripheral processors (Fig. 1, #120-150 and Page 4, lines 3-11) are the items that handle the methods of claim 1" and that "nowhere in the specification does it teach an implementation of the peripheral processors in any configuration that comprises a register set, and Fig. 1 seems to show that the PP are not." Applicants would again respectfully submit that the claims are to be interpreted according to their ordinary meaning unless found to be indefinite. As there are no outstanding claim rejections under 35 U.S.C. §112, Applicants submit that the Examiner's references to Applicants' specification are unnecessary and improper. Moreover, Applicants submit that the Examiner's cited portions of ***Muller*** teach, an input port process (IPP) 310, a packet memory 325, a control field 327, and an external shared memory 230 rather than "a register set" as claimed.

In the present Office Action, the Examiner states with respect to Applicants' claim 1 that, ***Muller*** teaches a method of packet processing comprising, "parsing a packet, said packet having a header portion, to determine a vector (Fig. 3, #310-320, and all proof listed above)"; "coordinating processing using said vector (Fig. 5, #515-520, Fig. 7)"; "deconstructing said packet header to form header data (col. 6, lines 5-10, where it is anticipated that the extraction of header data is a required first step to analysis of the aforementioned header data)"; "searching one or more data structures based on said header data to produce search results (col. 6, lines 26-32)"; "editing said packet based on said search results, said header data, and said vector (Fig. 3,

#330)"; wherein "said coordinating further comprises monitoring said deconstructing, said searching, and said editing (col. 3, lines 62-65)." Applicants respectfully disagree.

As previously discussed herein, Applicants respectfully submit that ***Muller*** (Fig. 3, #310-320, "and all proof listed above") fails to teach, show, or suggest, "parsing a packet, said packet having a header portion, to determine a vector" as claimed.

Applicants further submit that ***Muller*** (Column 6, Lines 26-32) fails to teach, show, or suggest, "searching one or more data structures based on said header data to produce search results" as claimed. Rather, the cited portion of ***Muller*** teaches that,

> In addition, for unicast routing, the IPP 310 replaces the destination address (DA) field with a DA supplied by the search engine 315. For example, this can simply be done using multiplexor logic to select either the original value found in the DA field or the DA value received from the search engine 315 based upon a DA replacement control signal issued by the search engine 315. For VLAN support, the IPP 310 selectively replaces or inserts the value in the VLAN tag field.

Applicants respectfully request that the Examiner describe more clearly and elaborate as to how the cited portion of ***Muller*** may be construed as teaching "searching" as claimed.

Applicants further submit that ***Muller*** (Fig. 3, #330) fails to teach, show, or suggest, "editing said packet based on said search results, said header data, and said vector" as claimed. Applicants submit that it is unclear how ***Muller*** can teach, "editing said packet based on said search results" when it is not accepted that or understood how ***Muller*** teaches, "searching one or more data structures" to produce the "search results" as previously described. Moreover, while ***Muller*** (Column 6, Line 66 – Column 7, Line 4) teaches that,

> The OPP 330, retrieves the packet and associated control field information from the packet memory 325 and, in response to the associated control field information, selectively modifies the input packet further as it is output to the MAC 335 and provides control information to the output MAC 335"

Muller further teaches (Column 2, Lines 14-20) that,

> In one embodiment, the control field information consists of a flag to indicate that the source address needs replacement. In another embodiment, the control field information consists of flags to indicate whether the packet came in tagged, the packet came in tagged but the tag was modified or that the packet is not to be tagged.

Consequently, Applicants respectfully submit that ***Muller*** fails to teach "editing said packet based on said search results, said header data, and said vector" as claimed (Applicants' claim 1, emphasis supplied).

As Applicants have demonstrated that ***Muller*** fails to teach, show, or suggest, "searching" and "editing" as claimed, it follows that ***Muller*** cannot be construed as teaching, "coordinating processing using said vector" where "said coordinating further comprises monitoring said deconstructing, said searching, and said editing" as claimed. (Applicants' claim 1, emphasis supplied) Moreover, it is unclear how the Examiner's cited portions of ***Muller*** (Fig. 5, #515-520, Fig. 7; Column 3, Lines 62-65) are intended by the Examiner to demonstrate such a teaching. Applicants respectfully request that the Examiner describe more clearly and elaborate as to how the cited portions of ***Muller*** may be construed as teaching "coordinating" as claimed.

In the present Office Action, the Examiner states with respect to Applicants' claim 6 that, ***Muller*** teaches an apparatus comprising, "a central processor for packet processing, said central processor comprising a register set (col. 3, lines 55-62)"; and "one or more peripheral processors each connected to said central processor an each comprising a register set (col. 3, lines 56-58)" wherein, "each said peripheral processor returns at least one datum to said central processor (Fig. 2)"; and "said central processor communicates with said peripheral processor (col. 3, lines 62-65). Applicants respectfully disagree.

Applicants respectfully submit that the Examiner has failed to address an element of Applicants' claim. More specifically, the Examiner has failed to point out whether, and if so, how, ***Muller***, or any of the other cited references, teach one or more peripheral processors comprising "a packet parser to determine a vector" as claimed. (Applicants' claim 6, as previously amended) Moreover, as discussed previously herein with respect to Applicants' claim 1, it is respectfully submitted that ***Muller*** fails to teach, show, or suggest a packet parser "to determine a vector" as claimed.

Applicants therefore respectfully submit that claims 1 and 6, are each independently allowable over the Examiner's cited reference, ***Muller***. Applicants' claims 15, 20, and 25, which include limitations substantially similar to those described with respect to Applicants' claim 1, and remaining claims 2-5, 7-14, 16-19, 21-24 and 26-29, which depend directly or indirectly from claims 1, 6, 15, 20 or 25, are similarly allowable for at least those reasons as stated for the

allowability of those claims. Accordingly, Applicants submit that the Examiner's rejections under 35 U.S.C. §102 and §103 are overcome, that all currently pending claims are allowable over the Examiner's cited references, and hereby request that the Examiner's rejections be withdrawn.

In the present Office Action, the Examiner notes that Applicants have not yet addressed the items of art added to reject the dependent claims. Applicants respectfully disagree. While Applicants have not explicitly addressed each of the Examiner's rejections, in the response dated November 13, 2002 Applicants indicated that they had elected to "overcome-in-part and respectfully disagree and traverse-in-part" the Examiner's rejections. It should be appreciated therefore that Applicants have not acquiesced to any of the Examiner's rejections. Additionally, as all rejections of dependent claims rely on the Examiner's rejection of claims 1-3, 6, 7, 13-17, 20-22, and 25-27 under 35 U.S.C. §102, Applicants respectfully submit that such rejections have been implicitly addressed and overcome. Applicants reserve the right to revisit and/or explicitly address any outstanding rejection at a later time.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nevertheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at (512) 439-5097.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box: AF, Commissioner for Patents, Washington, D.C. 20231, on 4-28-03.

Attorney for Applicant(s) — Date of Signature: 4-28-03

Respectfully submitted,

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